4BIT REAL TIME CLOCK MODULE with I/O CONNECTIONS

RTC-58321/58323

■ Overview

The RTC-58321/58323 is a CMOS real time clock modules with perpetual calendar function developed for microcomputer applications.

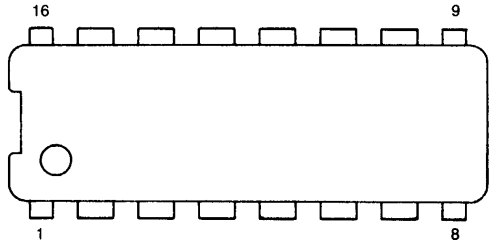
It has a built-in 32.768 kHz quartz resonator, and provides clock and calendar registers for year, month, day, day-of-week, hours, minutes and seconds, with 12-hour/24-hour selection, plus automatic leap-year correction with software selection for local calendars, and an additional periodic reference signal output.

Being a CMOS device, it has a very low power consumption for battery back-up purposes.

■ Features

- Adjustment-free built-in quartz resonator keeps component count low.
- Built-in clock and calendar registers for year, month, day, day-of-week, hours, minutes and seconds.
- 12-hour/24-hour selection.
- Automatic leap-year correction, with software selection for local calendars.
- Counter start, stop and reset functions.
- Periodic reference signal output selectable: 1024 Hz, or 1 second, 1 minute or 1 hour intervals.
- Data bus is 4-bit bi-directional, with memory-type reads and writes.
- CMOS device, for very low power consumption, and long battery back-up period.
- Compatible at pin and function levels with the MSM58321 RS.

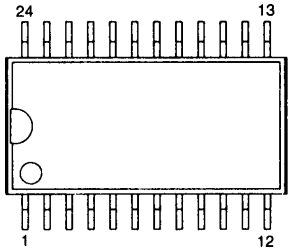
■ Pin connections



1. CS_2
2. WRITE
3. READ
4. D_0
5. D_1
6. D_2
7. D_3
8. GND
9. ADDRESS WRITE
10. $\overline{BUSY}$
11. STOP
12. TEST
13. CS_1

14 to 16. V_{DD}

✳Connect power supply positive side to pin 16.



1 to 4. NC

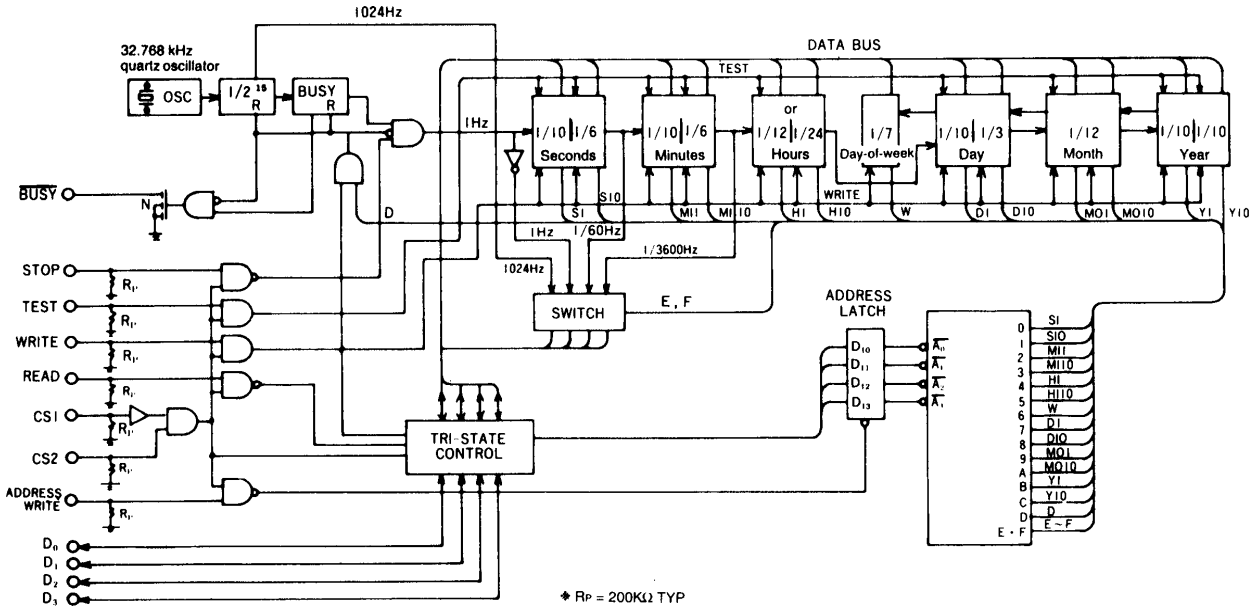
5. CS_2
6. WRITE
7. READ
8. D_0
9. D_1
10. D_2
11. D_3
12. GND
13. ADDRESS WRITE
14. $\overline{BUSY}$
15. STOP
16. TEST
17. CS_1

18 to 24. V_{DD}

NC: Pins are fixed low.

✳Connect power supply positive side to pin 24.

■ Block diagram



■ Pin functions

Pin numbers		Pin symbol	Input/output	Function
RTC-58321	RTC-58323			
1	5	CS_2	Input	Chip select. When high, device can be accessed.
2	6	WRITE	Input	Set high to write.
3	7	READ	Input	Set high to read.
4 to 7	8 to 11	D_0 to D_3	Both	Address/data bus.
8	12	GND		Negative power supply.
9	13	ADDRESS WRITE	Input	Address latch. Set high to latch address from D_0 to D_3.
10	14	$\overline{BUSY}$	Output	1 Hz output pin.
11	15	STOP	Input	1 Hz on/off control pin. When high, the 1 Hz signal is disabled, and the counter stopped.
12	16	TEST	Input	Increment pin for the counter. Normally this pin should be fixed low.
13	17	CS_1	Input	Connect to power down detection circuit. (Fix high if there is no power down detection circuit.) When CS_1 is low, chip cannot be accessed, regardless of state of CS_2.
*	1 to 4	NC		Fix low.
14 to 16	18 to 24	V_{DD}		Positive power supply (normally +5 V).

* A bypass capacitor (minimum 0.01 μF) must be connected between V_{DD} and GND, as close as possible.

■ Characteristics

1. Absolute maximum ratings

Item	Symbol	Conditions (Pins)	Rated Value		Unit
Power supply voltage	V_{DD}	Ta = 25ºC, V_{DD}-GND	-0.3 to +7.0		V
Input voltages	V_I	Ta = 25ºC input pins	-0.3 to V_{DD} +0.3		V
Output voltages	V_O	D_0 to D_3	-0.3 to V_{DD} +0.3		V
Storage temperature	T_{STG}	Temperature stored as separate item.	RTC-58321	-55 to +85	ºC
			RTC-58323	-55 to +125	ºC
Soldering temperature	T_{SOL}	RTC-58321	Maximum 260 ºC for up to 10 seconds (pins); package maximum 150 ºC.		
		RTC-58323	Maximum 260 ºC for up to 10 seconds (twice maximum), or maximum 230 ºC for up to three minutes.		

2. Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Notes
Power supply		V_{DD}	4.5	5.0	5.5	V	V_{DD}-GND
Data hold voltage *1		V_{DH}	2.2	-	5.5		
Operating temperature	RTC-58321	T_{OP}	-10	-	70	ºC	
	RTC-58323		-30	-	85		

*1 Data hold voltage: This is the range of power supply voltage for which the internal operation of the clock is guaranteed. I/O operations are not guaranteed.

3. Frequency characteristics

Item		Symbol	Conditions	Max.	Unit
Frequency tolerance	RTC-58321 A	$\Delta f/f_O$	Ta = 25ºC V_{DD} = 5.0V	± 10	ppm
	RTC-58321 B			± 50	
	RTC-58323			5 ± 20	
Aging		fa	Ta = 25ºC;V_{DD} = 5.0V;first year	± 5	ppm/y
Temperature characteristics *2		t_{OP}	V_{DD} = 5.0V;Ta = -10 to 70ºC	+ 10/-120	ppm
Voltage characteristics		f_V	V_{DD} = 2.2 to 5.5V Ta fixed, 5V reference	± 2	ppm

*2 Deviation from the frequency at 25 ºC.

Notes 1. Frequency tolerance based on V_{DD} = 5.0 V.
2. Frequency tolerance is value guaranteed on factory shipment.

4. DC characteristics

RTC-58321 (V_{DD} = 5V ± 0.5V, Ta = -10 to 70ºC)
RTC-58323 (V_{DD} = 5V ± 0.5V, Ta = -30 to 85ºC)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High input voltage	V_{IH1} *1			3.6			V
	V_{IH2} *2			V_{DD} - 0.5			V
Low input voltage	V_{IL}					0.8	V
Low output voltage	V_{OL}	I_{OL} = 1.6mA				0.4	V
Low output current	I_{OL}	V_{OL} = 0.4V		1.6			mA
High input current	I_{IH} *3	V_{IH} = 5V		10	30	80	µA
Low input current	I_{IL} *3	V_{IL} = 0V				-1	µA
Input leakage current	I_{LIH}	V_{IH} = 5V				1	µA
Input off-state leakage current	I_{LIL}	V_{IL} = 0V				-1	
Input capacity	C_I	f = 1MHz			5		pF
Current consumption	I_{OP}	V_{DD} = 5V	*4		100	500	µA
			*5		20	40	
		V_{DD} = 3V	*4		15	30	
			*5		7	20	
Oscillation start time *6	tosc	V_{DD} = 5V Ta = 25ºCºC			1.5	3.0	sec.

*1 Pins CS_2, WRITE, READ, ADDRESS WRITE, STOP, TEST and D_0 to D_3
*2 CS_1
*3 Pins CS_1, CS_2, WRITE, READ, ADDRESS WRITE, STOP and TEST
*4 CS_1 and CS_2 high, $\overline{BUSY}$ Open-circuit
*5 CS_1, CS_2 and $\overline{BUSY}$ Open-circuit
*6 Confirmed by $\overline{BUSY}$

5. AC characteristics

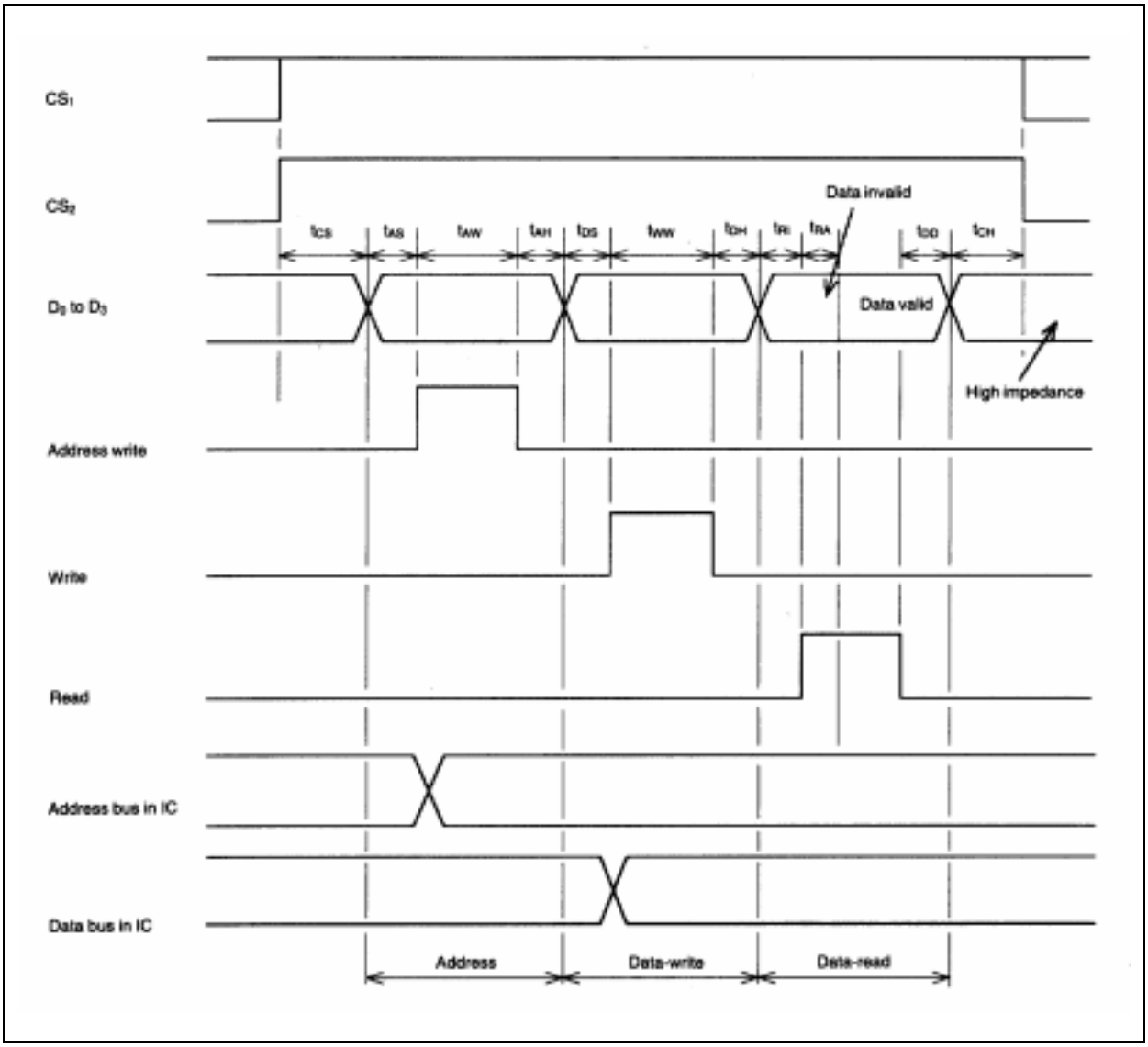
RTC-58321 (V_{DD} = 5V ± 0.5V, Ta = -10 to 70ºC)
RTC-58323 (V_{DD} = 5V ± 0.5V, Ta = -30 to 85ºC)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Chip select set-up time	t_{CS}	-	0	-	-	µS
Address set-up time	t_{AS}	-	0	-	-	µS
Address write pulse width	t_{AW}	-	0.5	-	-	µS
Address hold time	t_{AH}	-	0.1	-	-	µS
Data set-up time	t_{DS}	-	0	-	-	µS
Write pulse width	t_{WW}	-	2	-	-	µS
Data hold time	t_{DH}	-	0	-	-	µS
Read inhibit time	t_{RI}	-	0	-	-	µS
Read access time	t_{RA}	-	-	-	*	µS
Read delay time	t_{DD}	-	-	-	1	µS
Chip select hold time	t_{CH}	-	0	-	-	µS

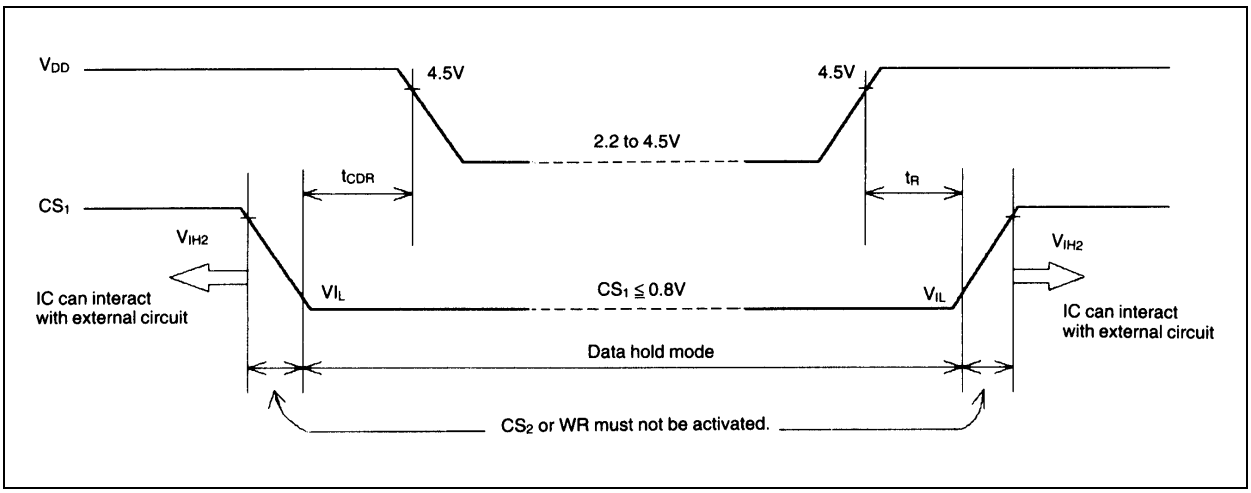
* $t_{RA} = 1\mu S + C \times R \times \ln \frac{V_{DD}}{V_{DD} - V_{Hmin}}$

C : capacitance of data line
R : pull-up resistance
V_{Hmin} : high voltage level of IC connected to data line
ln : natural logarithm

6. Timing chart



7. Data hold timing



■ Registers

1. Register table

Address (hexadecimal)	D_3 (A_3)	D_2 (A_2)	D_1 (A_1)	D_0 (A_0)	Register name	DATA D_3	DATA D_2	DATA D_1	DATA D_0	Count value	Notes
0	0	0	0	0	S_1	s_8	s_4	s_2	s_1	0 to 9	Seconds units register
1	0	0	0	1	S_0	*	s_{40}	s_{20}	s_{10}	0 to 5	Seconds tens register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 to 9	Minutes units register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 to 5	Minutes tens register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	0 to 9	Hours units register
5	0	1	0	1	H_{10}	24/12	pm/am	h_{20}	h_{10}	0 to 1 or 0 to 2	Hours tens register
6	0	1	1	0	W	*	w_4	w_2	w_1	0 to 6	Day-of-week register
7	0	1	1	1	D_1	d_8	d_4	d_2	d_1	0 to 9	Day units register
8	1	0	0	0	D_{10}	Leap year select		d_{20}	d_{10}	0 to 3	Day tens register
9	1	0	0	1	MO_1	mo_8	mo_4	mo_2	mo_1	0 to 9	Month units register
A	1	0	1	0	MO_{10}	*	*	*	mo_{10}	0 to 1	Month tens register
B	1	0	1	1	Y_1	y_8	y_4	y_2	y_1	0 to 9	Year units register
C	1	1	0	0	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 to 9	Year tens register
D	1	1	0	1		*	*	*	*		Reset register
E	1	1	1	0		1hour	1minute	1second	1024Hz		Reference signal registers
F	1	1	1	1							

2. Notes

(1) The device uses positive logic, and a logic high voltage corresponds to a 1 in a register bit.

(2) Do not set the clock to impossible dates (17:34 pm on February 30th, for example). The results are unpredictable.

(3) When the device is powered on, the initial settings of all bits are undefined.

■ Register functions

1. Date and time registers

(1) The register values are in BCD, and used positive logic.

E.g.(S_8, S_4, S_2, S_1) = (1, 0, 0, 1) = 9 seconds

(2) Day-of-week register

The value is coded as 0 to 6, with Sunday = 0.

Code	0	1	2	3	4	5	6
Day	Sun.	Mon.	Tue.	Wed.	Thud.	Fri.	Sat.

(3) pm/am, h_{20} and h_{10} registers

The range of these values depends on whether the 12-hour or 24-hour clock is being used.
The pm/am bit is used only when the 12-hour clock is selected.
Set D_3 to 1 for the 24-hour, and to 0 for the 12-hour clock.
Set D_2 to 1 for pm and to 0 for am. Writing a 1 to bit D_3 automatically resets bit D_2 to 0.

Selection	Value range
12-hour clock	12:00 to 11:59 am and pm *
24-hour clock	00:00 to 23:59

* Note: 12:00 am represents 12:00 midnight, and 12:00 pm represents 12:00 noon.

(4) Y1 and Y_{10} Leap year selection

Bits D_3 and D_2 of the day tens register select the year value module 4 to be used for leap years.

Calendar	D_3	D_2	Value module 4 for leap year
Standard calendar	0	0	0
	0	1	3
	1	0	2
	1	1	1

(5) Do not set the clock to impossible dates (17:34 pm on February 30th, for example). The results are unpredictable.

2. Reset register (Control register D)

Select this register to reset the last five stages of the $1/2^{15}$ divider, and the busy circuit.
Latch the hexadecimal value D using the ADDRESS LATCH pin, and set WRITE high to carry out the reset.

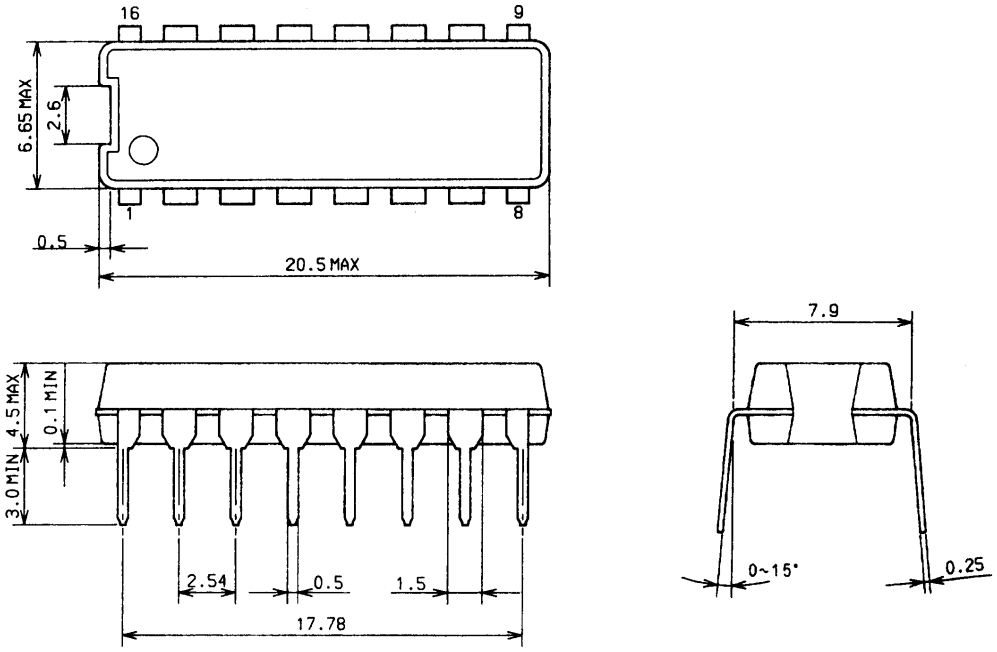
3. Reference signal (Control registers E and F)

Latch the hexadecimal value E or F using the ADDRESS LATCH pin, and set WRITE high to obtain the reference signal values on D_0 to D_3.

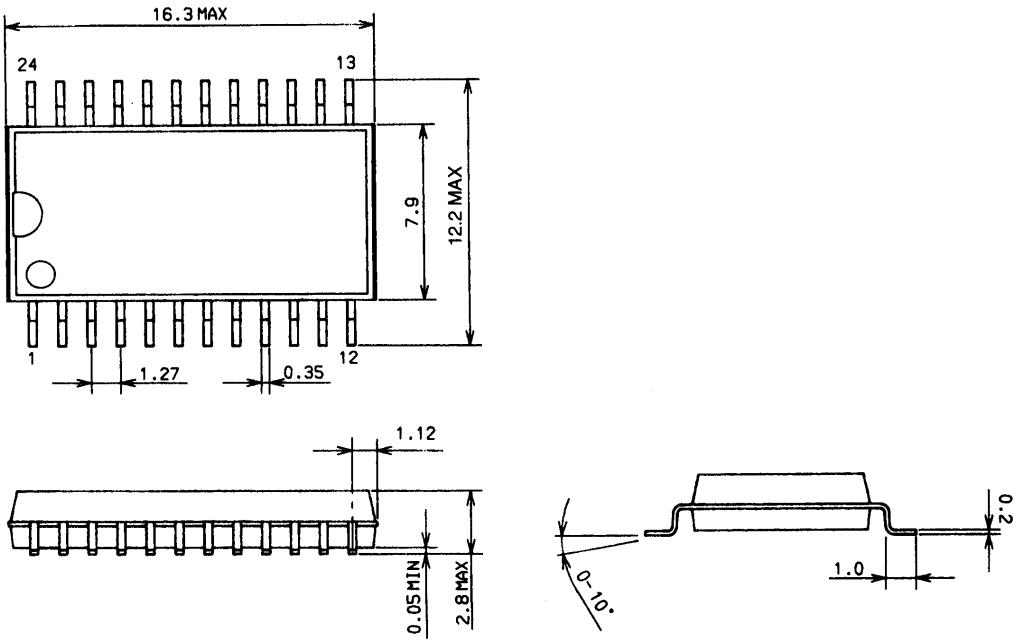
■ Package dimensions

(1) RTC-58321

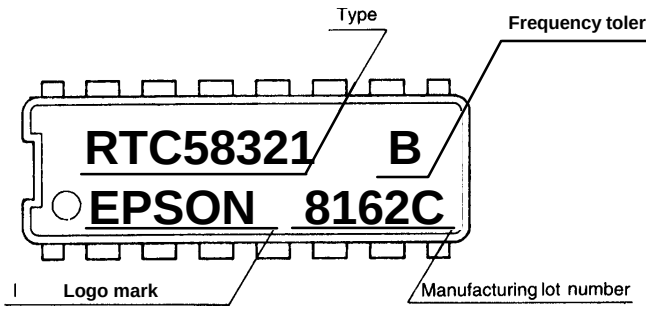
(Unit:mm)



(2) RTC-58323



■ Marking layout

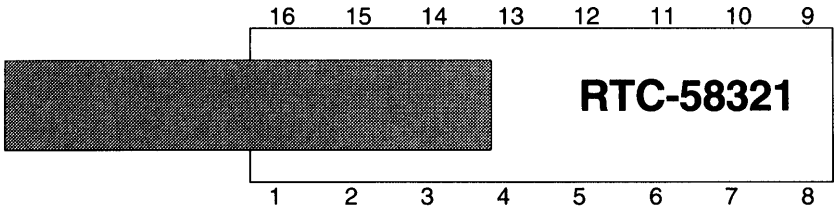


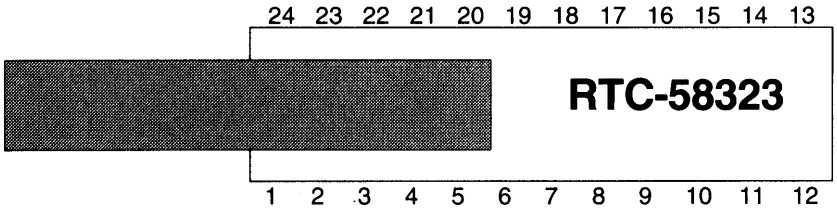
Type	Indication	Tolerances
RTC-58321	A	±10 ppm
	B	±50 ppm
RTC-58323		5 ±20 ppm

Note: The illustration is a general representation of the content and the location of information on the label, and is not a detailed specification of the typeface, size or positioning of printing used on the label.

■ Application notes

(1) In order to realize low-power operation, the device has a high impedance; the shaded portion in the figure below is highly susceptible to inductance effects, and should be kept clear of signal lines.





(2) Power supply filter capacitor
To ensure stable operation against transients and noise, connect a bypass capacitor of at least 0.01 μF (ceramic) across the power supply, close to the device.

(3) This device passes a drop test (from 75 cm onto a hard board), but it is possible for the crystal resonator to be damaged by the shocks produced by some mounting equipment. It is important to confirm that the mounting conditions for the equipment being used do not adversely affect performance. Re-check if any of the mounting conditions change.

(4) There is a possibility of damage to the crystal resonator during ultrasonic cleaning. Because of the wide variation of conditions in ultrasonic cleaning equipment, the performance of this device is not guaranteed if it is subject to ultrasonic cleaning.

(5) This is a CMOS device, and the standard precautions against static electricity should be taken.

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